August 23, 2002

TO: Commissioner of Patents and Trademarks
Washington, D.C. 20231

FROM: George O. Saile, Reg. No. 19,572
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SUBJECT:

Serial #:	09/587,465
File Date:	06/05/2000
Inventor:	LIN, JING-CHENG
Examiner:	SARKAR, ASOK K.
Art Unit:	2829
New Title:	METHOD OF FORMING MULTILAYER DIFFUSION BARRIER FOR COPPER

RESPONSE TO FINAL OFFICE ACTION

This is in response to the Final Office Action date mailed June 25, 2002. Please amend the above identified application for patent as follows:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on August 26, 2002.

Signature: Stephen B. Ackerman Date: 8/26/02

Stephen B. Ackerman, Reg. No. 37,761

REMARKS

Examiner Asok K. Sarkar is thanked for carefully examining and reviewing the subject patent application. The claims and the specifications have been amended in accordance with the Examiner's kind suggestions, and all claims are now believed to be in condition for allowance.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide an improved method of fabrication in the formation of an improved copper metal diffusion barrier layer having the structure, W/WSiN/WN, in single and dual damascene interconnect trench/contact via processing with 0.10 micron nodes for MOSFET and CMOS applications. The diffusion barrier is formed by depositing a tungsten nitride bottom layer, followed by an in situ SiH_4/NH_3 or SiH_4/H_2 soak forming a WSiN layer, and depositing a final top layer of tungsten. This invention is used to manufacture reliable metal interconnects and contact vias in the fabrication of MOSFET and CMOS devices for both logic and memory applications and the copper diffusion barrier formed, W/WSiN/WN, passes a stringent barrier thermal reliability test at 400 °C. Pure single barrier layers, i.e., single layer WN, exhibit copper punch

through or copper spiking during the stringent barrier thermal reliability test at 400 °C.

In summary of the present invention, a process flow description follows that summarizes the necessary process steps and sequence of steps necessary for the main embodiments of the present invention, to form W/WSiN/WN barrier layer, which exhibits high diffusion resistance to both copper and silicon (at both interfaces). The necessary process steps and sequence of steps necessary to form the W/WSiN/WN are outlined, as follows. Step one is the deposition of the WN film or layer in the trench/via opening by metal-organic chemical vapor deposition (MOCVD) from the reduction of tungsten organic precursors, or deposited by plasma-enhanced chemical vapor deposition (PECVD), or by physical vapor deposition (PVD), sputtering. Step two in the process flow description is the an in situ soak process treating the WN layer with a SiH_4/NH_3 gas mixture or a SiH_4/H_2 gas mixture, at between from about 300 to 400 °C. This reactive soak process forms a WSiN layer on top of the WN layer, thus a WSiN/WN barrier. Following the silane soak treatment, is step three, the final top barrier deposition by chemical vapor deposition (CVD) or physical vapor deposition

(PVD), sputtering, of a tungsten layer. Thus, a W/WSiN/WN barri r layer is formed. Next, step four is the copper seed layer deposition with improved adhesion and copper crystal texture, preferred dense <111>, upon the rigid diffusion the barrier layer, W/WSiN/WN. This fine crystal texture is important for subsequent electrochemical deposition (ECD) of copper, which subsequently fills the trench/via cavity. The copper seed layer, deposited over the tungsten layer, exhibits fine, highly dense grains, as studied by scanning electron microscopy (SEM). The subsequent process step, the electrochemical deposition (ECD) of copper, is used to fill the trench cavity, upon the copper seed layer. The kinetics of the electrochemical copper deposition process are based on a uniform, defect-free seed layer and barrier layer with good adhesion properties. The underlying layers improve and make wider the process window for the deposition of copper to fill both single and dual damascene structures.

The final processing step in building of the single and dual damascene structure is the chemical mechanical polishing (CMP) back of the excess electrochemical deposited copper metal. The copper is chem-mech polished back without dishing. In addition, any excess seed layer and barrier layer are

removed from the top substrate surface. The copper is polished back so that only the copper that lies in the openings is left to form single and dual inlaid structures that include via and interconnect portions. Device applications include MOSFET and CMOS devices.

CLAIM REJECTIONS - 35 USC 103:

The Examiner's objections to claims 1 - 10, 12 - 23, 25 and 26 under 35 USC 103(a), as being unpatentable over Edelstein et al.(US 6,181,012 B1, hereafter referred to as Edelstein), in view of Danek et al.(US 5,942,799, hereafter referred to as Danek), and Hsu et al.(US 6,194,310 B1, US 6,054,382, hereafter referred to as Hsu), are believed to be overcome, based on the following.

In reference to Edelstein, the main purpose and focus of Edelstein's invention is exactly as its title indicates, "COPPER INTERCONNECTION STRUCTURE INCORPORATING A METAL SEED LAYER." The focus is on forming copper alloys and other metals as seed layers. Most dual damascene processes for forming interconnection wiring incorporate metal diffusion barrier layers, as Edelstein's claim 25 states, "An interconnection system according to claim 24, wherein said diffusion barrier layer is deposited of a material selected from the group consisting of Ti, Ta, Nb, Mo, TaN, W, WN, TiN,

TaSiN, WSiN, TiAlN and TiSiN. Agree with Examiner that Edelstein fails to teach the method of the Applicant's invention, namely:

the formation of an improved copper metal diffusion barrier layer having the structure, W/WSiN/WN, in single and dual damascene interconnect trench/contact via processing with 0.10 micron nodes for MOSFET and CMOS applications. The diffusion barrier is formed by depositing a tungsten nitride, WN, bottom layer, followed by an in situ SiH_4/NH_3 or SiH_4/H_2 soak forming a WSiN layer, and depositing a final top layer of tungsten, W. It is not obvious exactly what barrier material or materials yield good adhesion and barrier properties, and enhances both copper seed deposition and copper electro-plating. In addition, it is not obvious exactly what processing conditions are optimum to achieve new and unexpected results.

In reference to Danek, the main purpose and focus of Danek's invention is to demonstrate the ease of deposition by a chemical vapor deposition, multi-station module or cluster tool. Applicant's invention teaches specifically the three component barrier layer: W/WSiN/WN, whereas Danek's invention teaches alternating layers of material (A) and material (B). In addition, Danek's invention does not c ntain

any claims to diffusion barrier compounds, elements, layers or material. See Danek, Claims 1 through 19. Danek's Figs. 1, 2, 4 and 6 are close to the Applicant's Invention, but do have significant differences from the Applicant's limited claims to the three component barrier layer: W/WSiN/WN.

The applicant's invention is different from Hsu's invention, in that, the Applicant's invention saves some processing steps. The Applicant's invention teaches a deposition of WN, bottom layer, then silane soak for WSiN, followed by deposition of W, top layer. Only two deposition steps are required, instead of three.

Also, Agree with the Examiner that Danek and Hsu fail to teach the Applicant's dual damascene process integration with a barrier layer.

Disagree with the Examiner, in that the Applicant's invention demonstrates diligence and reduction to practice in the processing conditions found in the depend claims. Also, there may exist similar process steps related to general semiconductor processing and dual damascene processing. There

are many common elements amongst the Prior Art that the Examiner has cited.

The Examiner's objections to claims 11 and 24 under 35 USC 103(a), as being unpatentable over Edelstein et al.(US 6,181,012 B1, hereafter referred to as Edelstein), in view of Danek et al.(US 5,942,799, hereafter referred to as Danek), and Hsu et al.(US 6,194,310 B1, US 6,054,382, hereafter referred to as Hsu), as applied to claims 1 and 14 above, and further in view of Yu et al.(US 6,291,332 B1) and Hsu et al.(US 6,054,382) are believed to be overcome, based on the following.

In reference to Yu, as the title of the invention states, "Electroless Plated Semiconductor Vias and Channels," Yu teaches a plating method for dual damascene. Yu's Column 2, line 28 to 40, emphasizes the need for the copper seed layer to have <111> crystal orientation, as the Applicant's invention achieves. Yu's claim 6 mentions some common barrier layer materials, with elemental W being the only material common to just one layer of the Applicant's invention.

In regards to the Examiner's obj ctions to the Applicant's claim 11 and 24 referencing the formation of fine grained <111> plated Cu, as being obvious over Edelstein, in view of Danek and Hsu, and further in view of Yu and Hsu, are believed to be overcome, based on the following.

Agree with the Examiner that fine grain <111> for seed and plated copper is desirable, but by what methods, can one achieve a <111> copper seed layer consistently and reliably on a dual damascene barrier layer. The Applicant's invention demonstrates the development of a process that achieves good properties in the seed and plated copper, and that has passed stringent reliability tests for copper interconnect wiring.

The Examiner's objections to claims 1 - 13 under 35 USC 103(a), as being unpatentable over Edelstein et al.(US 6,181,012 B1, hereafter referred to as Edelstein), in view of Koyama et al.(US 5,990,008, hereafter referred to as Koyama), are believed to be overcome, based on the following.

In Koyama's invention, with reference to column 7, lines 4 - 17, "W is used as the first layer, a second layer of WSiN may be used." Acknowledge the Examiner's remarks that Koyama

teaches a just a dual barrier layer. This is substantially different from the Applicant's invention, which a deposition of WN, bottom layer, then silane soak, followed by deposition of W, top layer. Only two deposition steps are required, instead of three. The sequence, selection of material and processing of the Applicant's invention are critical for good adhesion properties, good <111> copper plating and good electrical properties of the inlaid plated copper interconnects.

In Addition, Koyama claims only two material layers for the barrier layer, namely Ti and TiN, please see Koyama's Claims 9,10, 19,20, 29,30, 39 and 40.

In conclusion, for state-of-the-art advanced applications in silicon technology, the Applicant's invention is believed to be patentable over these various references, because there seems to be insufficient basis for concluding that the modification of Prior Art disclosures would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is

desirable. We believe that there is no such basis for the combination.

FINAL REMARKS

The Examiner Asok K. Sarkar is again thanked for carefully examining and reviewing the subject patent application. The specifications and claims have been reviewed in accordance with all the Examiner's kind suggestions, and after amending the specifications and claims in accordance with the Examiner's helpful suggestions, all claims are now believed to be in condition for allowance.

All rejected Claims 1 - 26 are now believed to be in allowable condition, and allowance is so requested.

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (845) 452-5863.

Respectfully submitted,

Stephen B. Ackerman, Reg. No. 37,761